Lunch: 12:15, Diner: 6pm
Introduction: Everybody uses 2 slides to present her/himself & to identify urgent questions for the seminar
Talks: up to 30 minutes plus 30 minutes of discussion

	Monday **Design**	Tuesday **Fault models & Metrics I**	Wednesday **Engines I**	Thursday **Engines II + Metrics II**	Friday **Lessons learned**
9 am	Welcome, ***Introducing everybody -> 2 slides presented by everyone!*** Anand Raghunathan, Kaushik Roy: ***Approximate Computing - Embracing Unreliability for Efficient Computing***	Suddhakar M. Reddy: ***Gracefully Degradable Higher Performance Systems*** Carsten Gebauer: ***Issues with applying fault tolerance in safety critical automotive applications***	Ravishankar K. Iyer: ***Experimental Validation of Computer Systems Dependability*** Bernd Becker, Matthias Sauer: ***Improving reliability by improving ATPG accuracy***	Cecile Braunstein: ***A Symbolic Model-Checking Framework for Transient Fault Robustness Classification and Quantification*** Jie Han: ***Stochastic Computational Approaches for Accurate and Efficient Reliability Evaluation***	Panel: ***(Fault models)***
10:30 am	John P. Hayes: ***Stochastic Computing Revisited*** Adit Singh: ***The Reliability Challenge from Variability Induced Timing Errors***	Matteo Sonza Reorda: ***Functional test: which role in real practice?*** Mehdi B. Tahoori: ***Wearout Modeling and Mitigation at Higher Levels of Abstraction***	Bodo Hoppe: ***Verifying archtiectural compliant recovery*** Massimo Violante: ***Validating fault tolerant designs in SRAM-based FPGAs: how to keep the route in an ocean of bits***	Marcela Simkova: ***Towards Beneficial Hardware Acceleration of Functional Verification*** Rolf Drechsler: ***Completeness-Driven Development***	Wrap-up-Panel
1:30 pm	Michael Orshansky: ***When Perfect is the Enemy of Efficient: Using Controlled Errors in Approximate Computing*** Ilia Polian: ***Towards a Cross-Layer Strategy Against Fault-based Attacks***	Eli Arbel: ***Reliability closure – how can we do better?*** Sachin Sapatnekar: ***How does device-level reliability affect my system?***	Excursion & dinner outside	Laurence Pierre: ***On the use of semi-formal methods for reliability analysis (at RT and TLM abstraction levels)*** *Jacob A. Abraham:* ***Software-level Fault Injection: an Effective Approach to Validating System Reliability***	Departure
3:00 pm	Masahiro Fujita: ***Error Tolerance and Engineering Change with Partially Programmable Circuits and their SAT-Based Programming*** Tomohiro Yoneda: ***Designing a Dependable Network-on-Chip Platform for Automotive Applications***	Ulf Schlichtmann: ***How to efficiently analyze aging effects in large circuits - and some ideas how to use the results*** Yasuo Sato: ***Analysis of Field Test Effectiveness to LSI Reliability***		*Shawn Blanton:* ***On-Chip Diagnosis*** Yoshiki Kinoshita: ***Validating Open Systems Dependability***	
4:30 pm	Panel: ***Beyond the limitations of approximate and statistical computing*** J.P. Hayes, M. Orshansky, A. Raghunathan, S. Sapatnekar	Panel: ***What's most urgent in industry?*** E. Arbel, (C. Gebauer), B. Hoppe, Y. Sato		Panel: ***(Engines & Metrics)***	