

# Dagstuhl Seminar 06141

## Dynamically Reconfigurable Architectures

April 02 - 07, 2006

organized by

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# Monday: Reconfigurability in Embedded Computing

- 09:00 Jürgen Becker, Gordon Brebner, Peter Athanas, *Jürgen Teich*  
**Welcome + Introduction**
- 10:00 Coffee break
- Chair Jürgen Becker*
- 10:30 Michael Hübner, Katarina Paulsson, Jürgen Becker  
**Physical 2D Morphware and Power Reduction Methods for Everyone**
- 11:00 Philip Leong  
**Floating Point FPGAs**
- 11:30 Walter Stechele  
**Dynamically Reconfigurable Systems-on-Chip: Autovision**
- 12:15 Lunch
- 14:00 Christian Hochberger  
**AMIDAR – A New Model for Adaptive Processors**
- 14:30 Thilo Pionteck, Erik Maehle  
**DynaCORE: Dynamically adaptable COprocessor based on REconfiguration**
- 15:00 Stamatis Vassiliadis  
**PISC: Polymorphic instruction Set Processors**
- 15:30 Coffee Break
- 16:00 Dietmar Fey  
**Technological Aspects for 3D FPGA architectures with optoelectronic interconnects**
- 16:30 Jan van der Veen, Jürgen Teich  
**ReCoLib**
- 17:00 *Breakout Session: Library for Applications Requiring/Supporting Reconfigurability*
- 18:00 Dinner

# Tuesday: Reconfigurability for Embedded and HPC

## *Chair Jürgen Becker*

- 09:00 Wolfgang Rosenstiel  
**Dynamically Reconfigurable Processor-Like Architectures**
- 09:30 Gerard Smit  
**Efficient Reconfigurable Architectures for streaming DSP applications**
- 10:00 David Kearney  
**Managing power amongst a group of networked embedded FPGAs using dynamic reconfiguration and task migration**
- 10:30 Coffee Break
- 11:00 Norbert Wehn  
**A Reconfigurable Outer Modem Platform for Future Communications Systems**
- 11:30 Doug Maskell  
**Pre-Routed FPGA Cores for Rapid System Construction in a Dynamic Reconfigurable System**
- 12:15 Lunch

## *Chair Peter Athanas*

- 14:00 Peter Zipf, Manfred Glesner  
**Towards an Automated Design of Application-specific Reconfigurable Logic**
- 14:30 Andreas Herkersdorf  
**Reconfiguration of Functionality versus Reconfiguration of Interconnect**
- 15:00 John Snowdon  
**Maintaining or Breaking Moore's Law**
- 15:30 Coffee break
- 16:00 Bernd Klauer  
**Superscalar Technology for Reconfigurable Computers**
- 16:30 Rainer Buchty, Wolfgang Karl  
**Reconfigurable Architectures and Instruction Sets**
- 18:00 Dinner

# Wednesday: New thoughts in RC

*Chair Gordon Brebner*

09:00

Gordon Brebner

**Dynamically Adaptable Behaviours (?)**

09:45

Peter Athanas

**FPGA Supercomputing**

10:25

Coffee break

10:55

Hartmut Schmeck

**Implications of Organic Computing for Reconfigurable Computing**

11:35

Reiner Hartenstein

**Reconfigurable Supercomputing: What are the Problems?**

12:15

Lunch

13:00

Hike Hochwaldalm

18:00

Dinner

20:00

*Breakout Session: Usefulness of Dynamic Reconfiguration*

# Thursday: Gap between Tools and Technology

*Chair Jürgen Teich*

- 09:00 Neil Bergmann  
**HW/SW Codesign for Reconfigurable System-on-Chip using a Process Model**
- 09:30 Roger Woods  
**Implementing High-Performance DSP Systems on Heterogeneous Programmable Platforms**
- 10:00 Oliver Diessel, Shannon Koh  
**Enabling RTR for Industry**
- 10:30 Coffee break
- 11:00 Andreas Koch  
**Back-End Issues in Hardware/Software-Compilation**
- 11:30 Klaus Waldschmidt  
**Reliability-Aware Power Management of Multi-Core Processors in modern (reconf.) System-on-Chips**
- 12:15 Lunch
- 14:00 Mateusz Majer, Diana Göhringer, Jürgen Teich  
**Bridging the Gap between Relocatability and Available Technology: The Erlangen Slot Machine**
- 14:30 Vincent Mooney  
**Design of a Hardware/Software RTOS for FPGAs with Processors**
- 15:00 Marco Platzner  
**Mapping Periodic Real-Time Tasks to Reconfigurable Hardware**
- 15:30 Coffee Break
- 16:00 Florian Dittmann, Franz Rammig  
**Reconfiguration Time Aware Processing on FPGAs**
- 18:00 Dinner
- 20:00 *Breakout Session: Reconfigurable Interconnect*

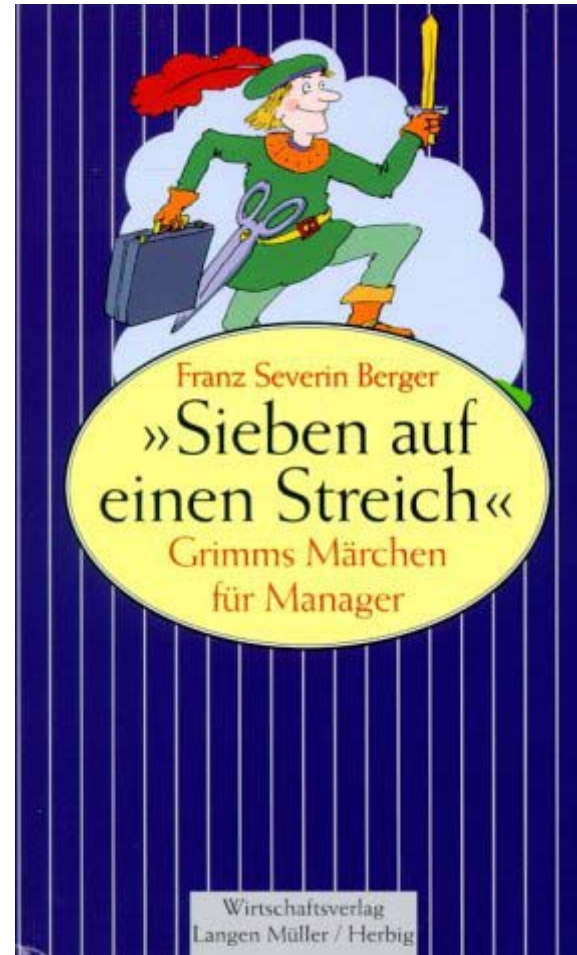
# Friday: Industrial Applications and Future Ideas

*Chair TBD*

- 09:00 Christophe Bobda  
**Adaptive On-Chip Multiprocessing**
- 09:30 Mladen Berekovic  
**The ADRES coarse-grained reconfigurable Array Processor**
- 10:00 Sven Heithecker, Amilcar Lucas, Rolf Ernst  
**FlexFilm: QoS-capable scheduling SDRAM controller**
- 10:30 Coffee break
- 10:45 Martin Middendorf  
**Multi-level Reconfigurable Architectures – The Switch Model**
- 11:15 Jozsef Vasarhelyi  
**Mojette Transform implementation on reconfigurable hardware**
- 11:45 Wrap Up and Close of Workshop
- 12:15 Lunch

# Questions (revisited)

- **Dynamic Reconfiguration (Wednesday Breakout Session)**
  - Needed?
  - Testability?
  - Reconfiguration Speed Requirements?
  - Overhead
  - Benefits: Better performance, smaller area, lower power
  - Applications requiring/benefiting from dynamic reconfiguration:  
**„Seven by one stroke!“**  
(Andreas Koch)



# Questions (revisited)



- **“Seven by one stroke!”**
  1. Video Processing (Grass Valley: mixing, denoising, color correction)
  2. Radar Tracking Modes
  3. Medical Imaging (Philips Medical: Real Time X-Ray)
  4. Software Defined Secure Radio (Harris)
  5. Multi-Standard Software Receiver (Atmel: DAB, DRM)
  6. Cognitive Radio (Thales: find free gaps in spectrum for own transmissions)
  7. OFDM Adaptive Filter (match filter capabilities to environment)

# Questions (revisited)

- **HPC (well) supported by FPGAs? No (Peter's talk)**
  - Floating Point
  - Clock rates
  - Energy efficiency?
- **Power**
  - Energy Consumption Problem?
  - Competitiveness w.r.t. to ASICs can be reached?
- **Libraries (Monday Breakout Session)**
  - ReCoLib ([www.r-space.de](http://www.r-space.de))
  - Must have data structures for a) modules and b) benchmarks

# Questions (revisited)

- **Architectures (Thursday Breakout Session)**

- Interconnect Granularity?
- Optical interconnect ready?
- Fine/Coarse grain?
- Functional units vs. Interconnect reconfigurability

- **Tools**

- Abstraction level /Specification language needed for expressing reconfigurability?
- Design Flow for RC?  
Stability, Support
- CAD with small runtime/memory reconfiguration