Low Level Compiler for XMONARCH

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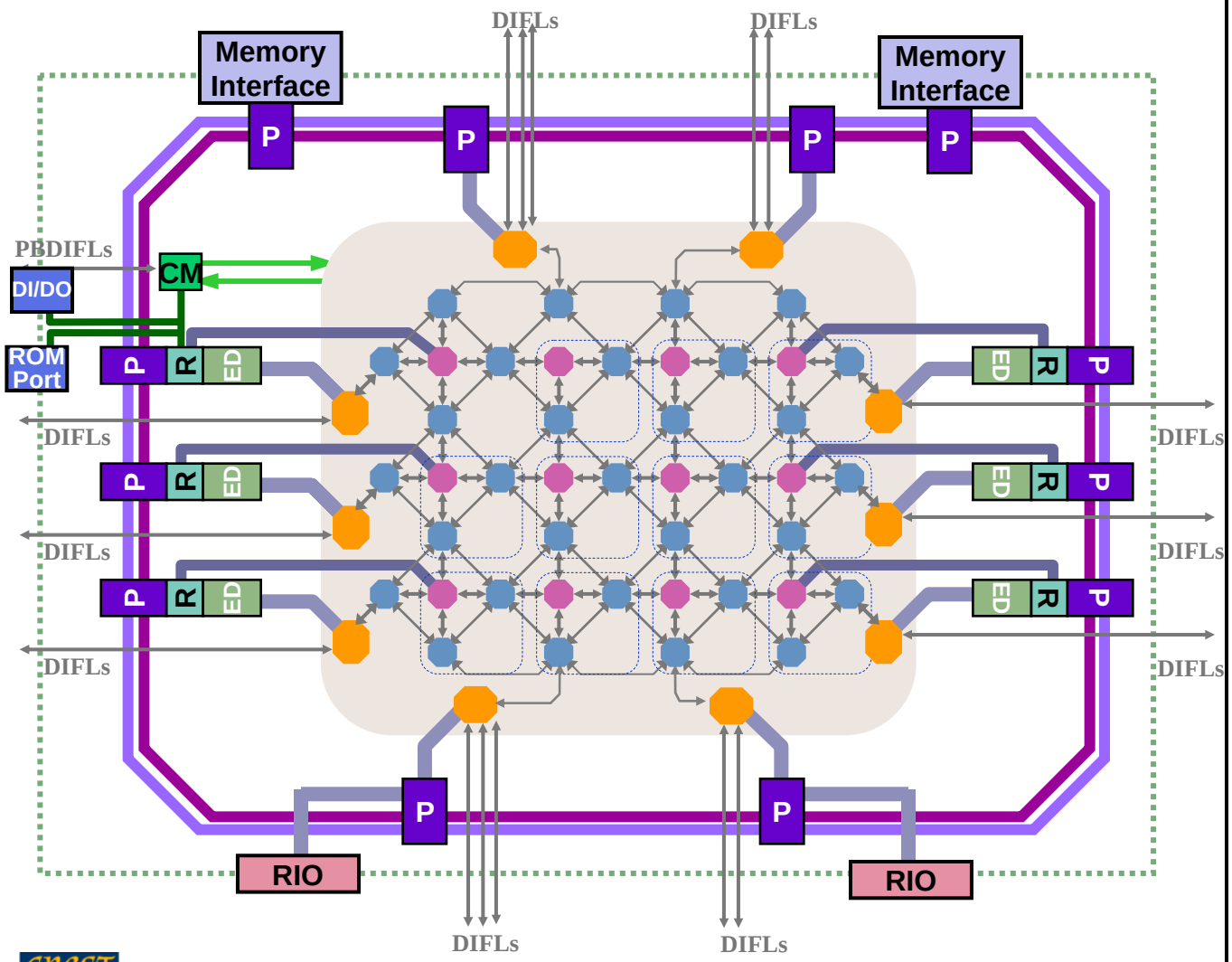
Outline

- MONARCH Chip Architecture
- XMONARCH Goals
- Compilation Flow
- Constructive Plan
- External Interfaces
  - SCE
  - HLC

MONARCH Chip Overview

Rev 12-Mar-06



- **Throughput 64 GOPS peak**
- **Multiple programming modes**
  - Reconfigurable, data flow
  - RISC scalar
  - RISC SIMD (Altivec-like)
- **90 nm bulk CMOS**
- **Clock 333 MHz**
- **Power 3-6 GFLOPS/W**
- **12 Arithmetic Clusters**
  - 96 adders (32 bits) fixed and float
  - 96 multipliers
- **31 Memory Clusters**
  - 124 dual port memories
  - 256W x 32 bits each (128KB)
  - 248 address generators
- **>72 DMA engines**
- **6 RISC processors**
- **12 MBytes on chip DRAM**
- **2 Bulk memory interfaces (8 GB/s BW)**
- **2 RapidIO (serial) interface**
- **17 DIFL ports (2.6 GB/s ea)**
- **On-chip ring 40 GB/s**

DIFL =Differential Inter FPCA Link

XMONARCH Dataflow Compiler: Goals

- **Design and implement C language-based (SVM) compiler for the MONARCH dataflow fabric**
  - **Compile application kernels implemented according to the Morphware Forum C-based Streaming Virtual Machine API (SVM) specification**
  - **Define interactions with MONARCH software development flows**
    - **Mercury SCE**
    - **Reservoir Labs High Level Compiler**
- **Develop an optimization framework**
  - **Recognize and optimize operations unique to the fabric**
  - **Target performance *at least* comparable to manually tuned code**

XMONARCH Optimizing Compiler: Goals

- Extend compilation to code generation for the RISC and Wide Word (WW) engines in MONARCH
  - Compilation and optimization of streaming kernels
  - Extensions for the RISC and WW engines
  - Cross-boundary (RISC/WW/fabric) optimization
  - gcc ABI compatible
- Additional high level and machine specific optimizations
- Focus on productivity, robustness, stability
  - IDE and graphical interface to MONARCH simulator
  - Rapid prototyping tools for developing streaming kernels
  - Enhance regression test suite
- Retarget to the MONARCH chip
- Interface with external development flows
  - Mercury SCE component authoring tools
  - Reservoir HLC

XMONARCH Compilation Flow

SVM Program

Partitioner

Front-end

Lower IR

Kernel Control Code

Explicitly Parallel Instruction Computing (EPIC) parametric Intermediate Representation

REBEL IR

Prototyping Tools

Remix

MDFG

Dataflow Backend

MONARCH Intermediate Representation

RISC/WW Backend

Back-end

IDE

Debugging Interfaces

Simulation & Visualization

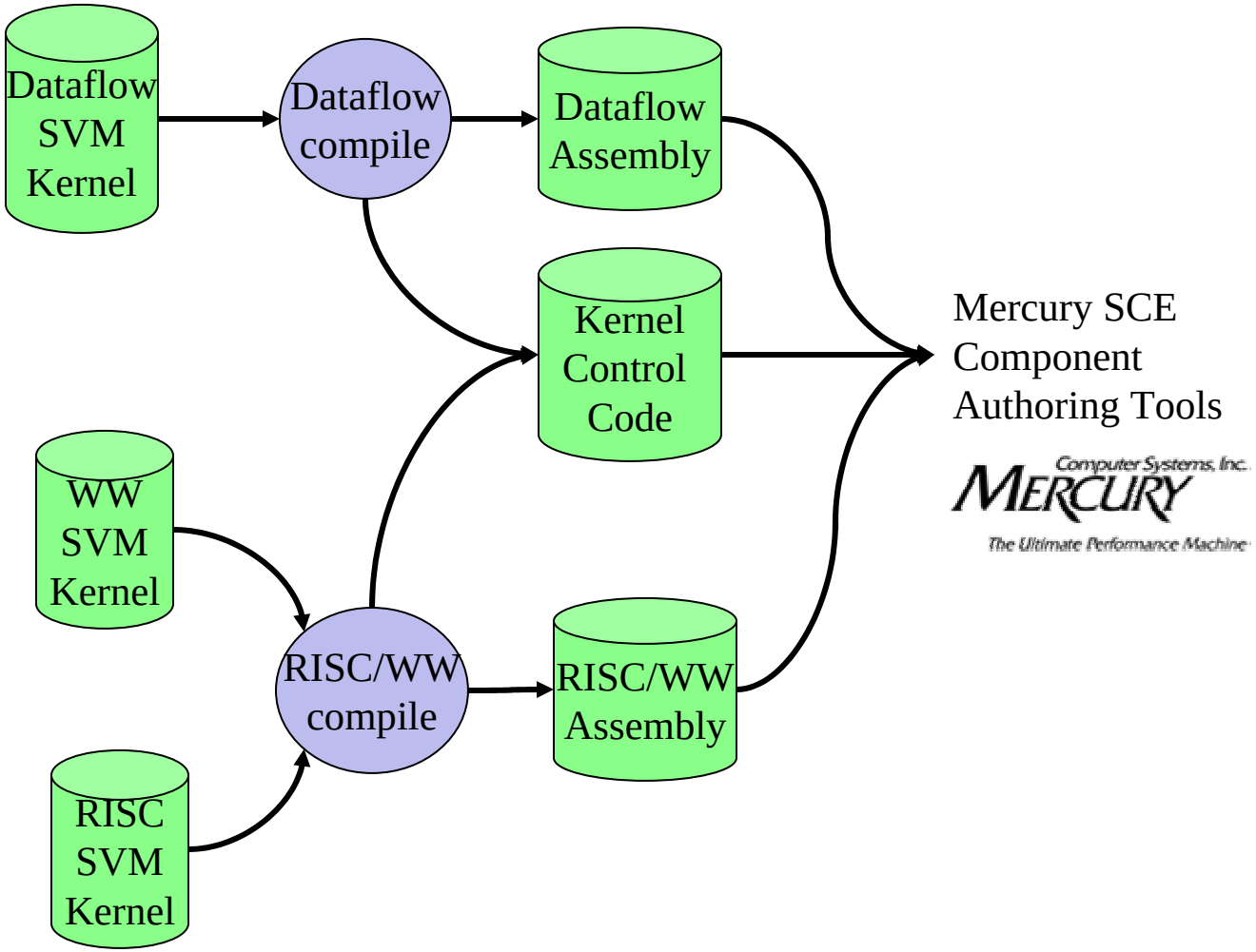
*.asm (dataflow)

*.asm (RISC/WW)

XMONARCH Optimizing Compiler: Constructive Plan

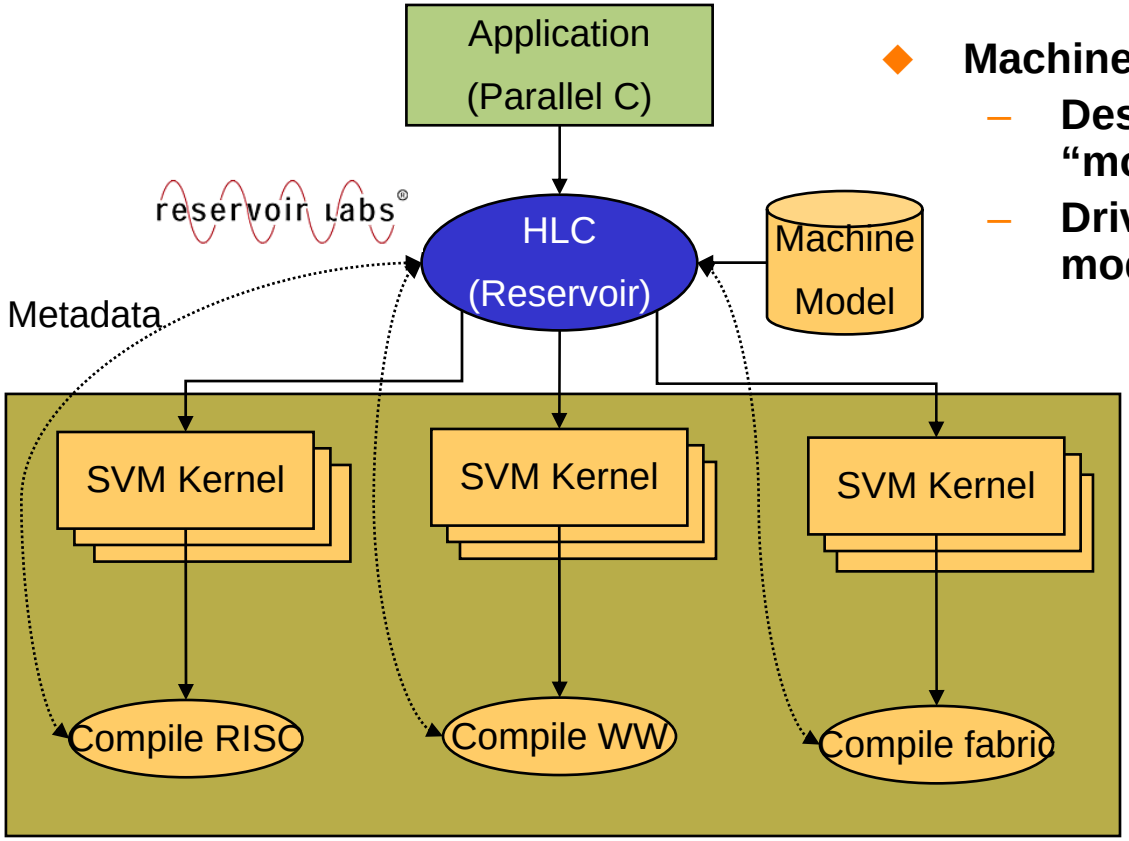
- **Core Compiler**
  - Leverage existing frameworks
    - Trimaran, Exogi libraries
  - Implement / port Trimaran modules to RISC ISA
    - Scheduling, Register Allocation, & Code Generation
  - Implement code generation for WideWord processor
  - Implement cross-target optimizations (RISC / WW / fabric)
- **Stability and Testing**
  - Industrial regression testing framework
  - Extend existing dataflow LLC regression test suite
  - Integrated (team) formal bug/issue tracking software
- **Productivity, Visualization, and Debugging**
  - Implement Python-based dataflow prototyping language
  - Implement Eclipse-based GUI for visualization
    - Implement plug-ins for MDFG simulator, fabric simulator, and integrated MONARCH simulator
- **External interfaces and prototype chip porting**
  - Interface with HLC and SCE teams
  - Retarget compiler framework to development board

Interoperation with the Mercury SCE Environment



- **Establish vocabulary for SCE metadata to be produced by Trimaran**

Interoperation with the Reservoir High Level Compiler (HLC)



- **Machine Model**
  - **Describe MONARCH "morphs"**
  - **Drive HLC cost models**

Metadata Interface

Capture program information

Vehicle for Feedback to HLC, e.g. feasibility (fabric), performance (area/time)