

Superscalar Technology for Reconfigurable Processors

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Outline

- Introduction
- Proposal: A superscalar architecture with a reconfigurable execution stage
- Simulation and Benchmarking
- FPGA-Implementation
- Conclusions



Introduction



Target of our work was to design a processor with the following features:

- All-purpose functionality
- Increased performance only by reconfiguration
- Compatibility with legacy processors with the same ISA
 - Existing compiler technology should be applicable
 - Legacy (program) code should run on the processor



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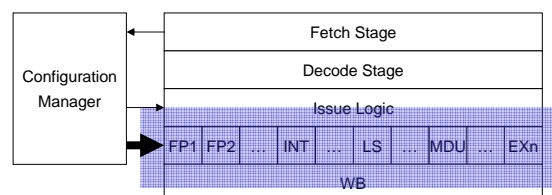
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Basic Ideas

- **Superscalar Architectures perform out-of-order execution**
 - based on the availability of unemployed FUs
 - based on the availability of executable instructions
- **Executable Instructions are scheduled and routed to free functional units by an issue logic**
- **Processors with different execution stages can execute the same code with different performance results.**
- **Subject of reconfiguration in the proposed architecture is the execution stage.**



Basic Ideas



Implementation



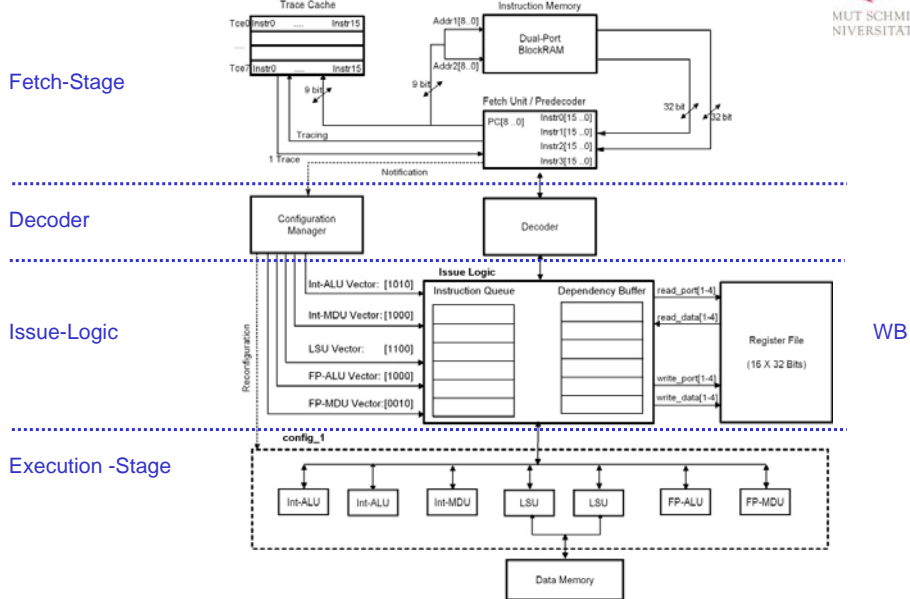
- ISA: Arm Thumb
- Target FPGA: Virtex-II-XC2V8000



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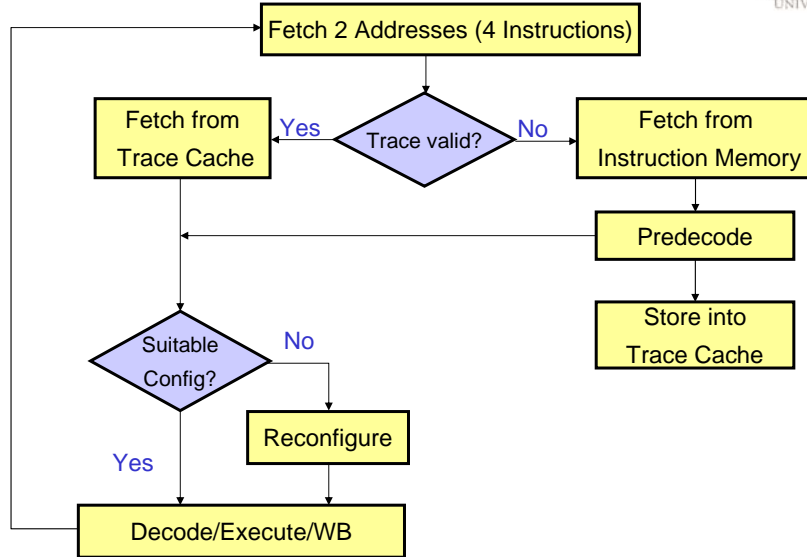
Implementation



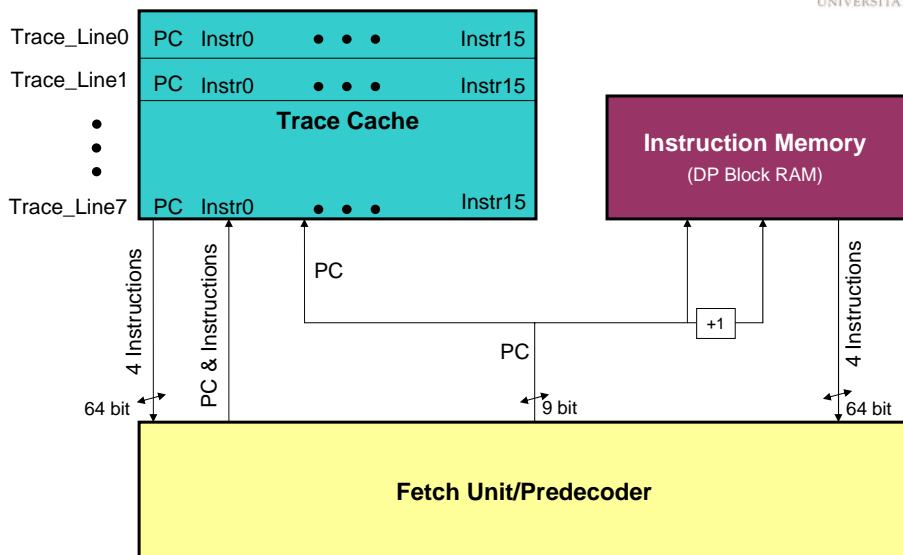
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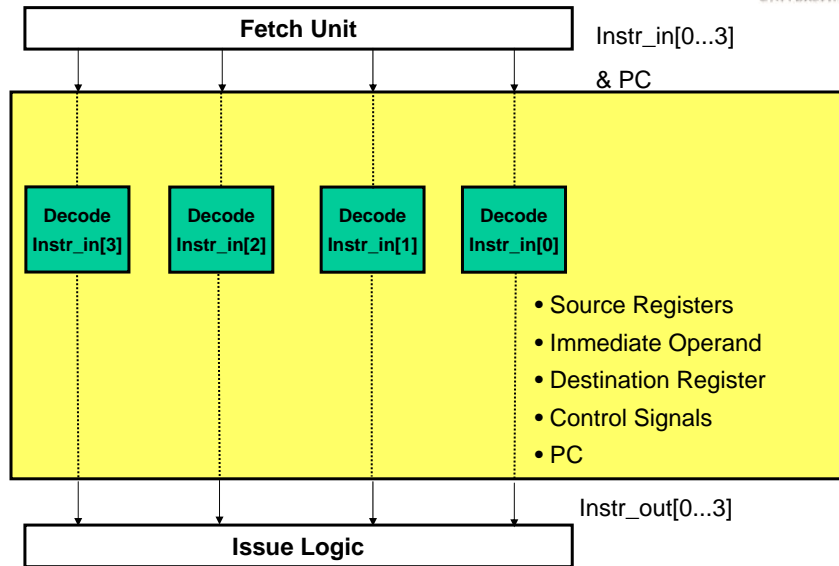
Operational principle



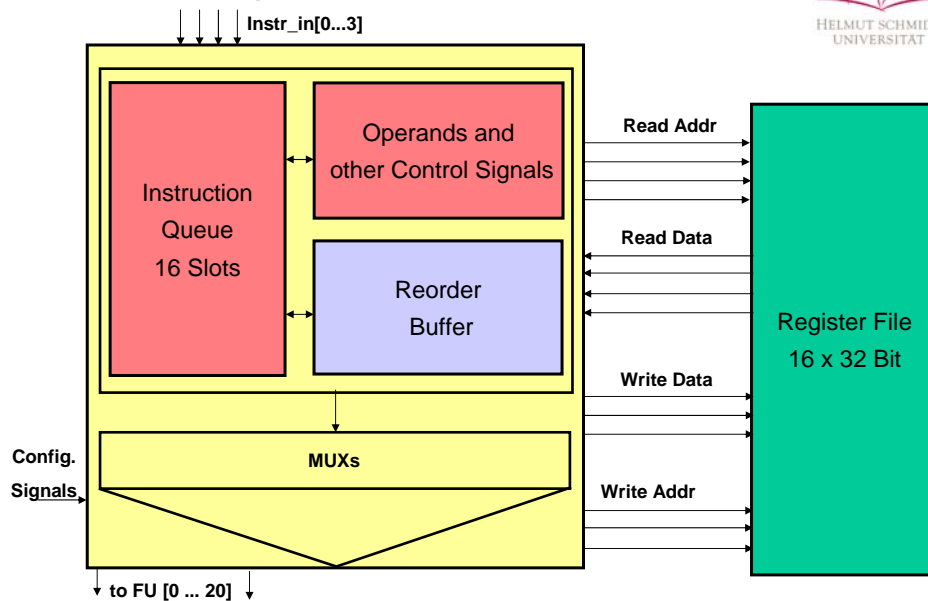
The fetch stage



The Decoder Stage



The Issue Logic



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Why Simulation ?



- Benchmarking with the SPEC CPU 2000 BM.
- Operating system support (File System, I/O, etc.)



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Simulation



- **Simulator:** ARM-Version of the SimpleScalar Toolset extended by:
 - a Trace Cache
 - the Configuration Manager
 - an extended issue-logic
 - a reconfigurable EX stage
- **Problems investigated:** Applications from the SPEC CPU2000 Benchmark
 - gzip: Datacompression
 - vpr: FPGA-Place & Route
 - gcc: GNU C Compiler
 - equake: Earthquake-Simulations
 - ammp: Chemical Computations
- **C-Compiler:** gcc



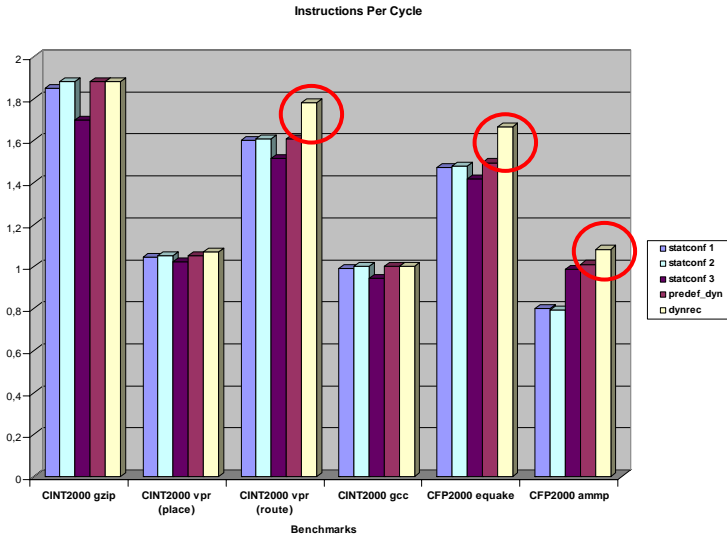
Hardware (Re)configuration Models



		Int-ALU	Int-MDU	LSU	FP-ALU	FP-MDU
statconf 1		2	1	2	1	1
statconf 2		4	2	4	1	1
statconf 3		2	1	4	2	2
predef_dyn	config1	2	1	2	1	1
	config2	4	2	4	1	1
	config3	2	1	4	2	2
dynrec		0 - 4	0 - 4	0 - 4	0 - 4	0 - 4



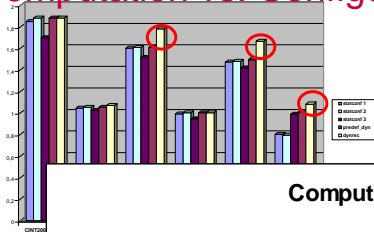
Instructions per Cycle (IPC)



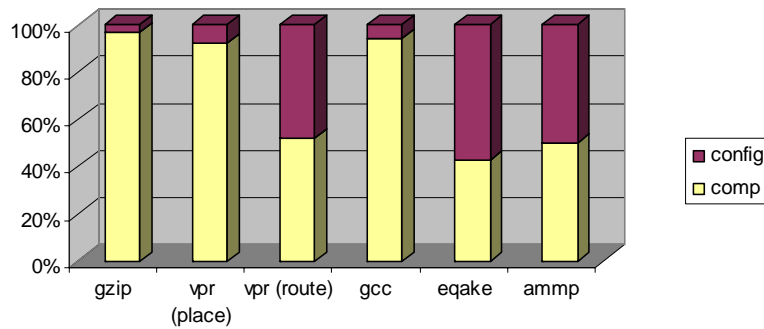
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Computation vs. Configuration



Computation/Configuration Ratio



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Hardware (Re)configuration Models



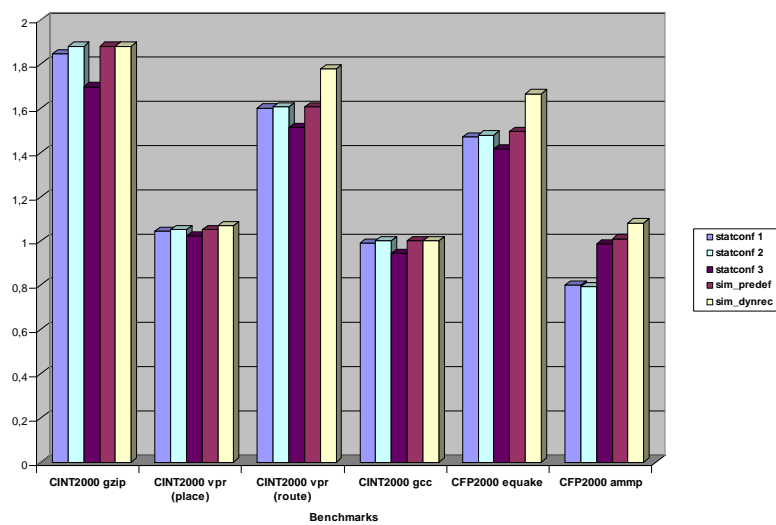
		Int-ALU	Int-MDU	LSU	FP-ALU	FP-MDU
statconf 1		4	1	2	4	1
statconf 2		8	4	4	1	1
statconf 3		2	1	4	4	4
predef_dyn	config1	4	1	2	4	1
	config2	8	4	4	1	1
	config3	2	1	4	4	4
dyn-rec		1 - 8	1 - 8	1 - 8	1 - 8	1 - 8



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Instructions per Cycle (IPC)



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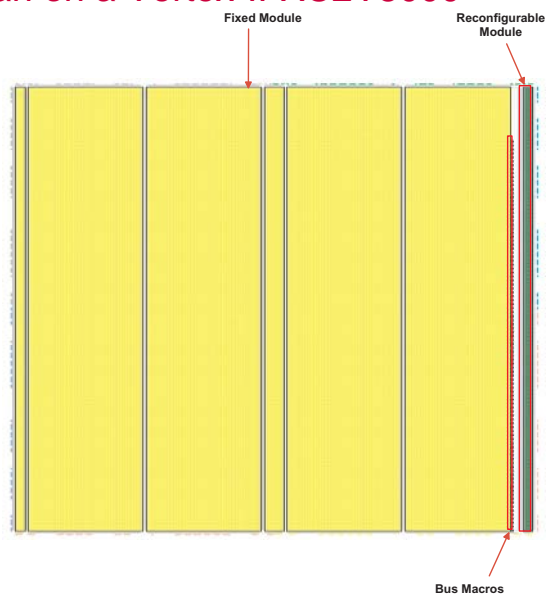
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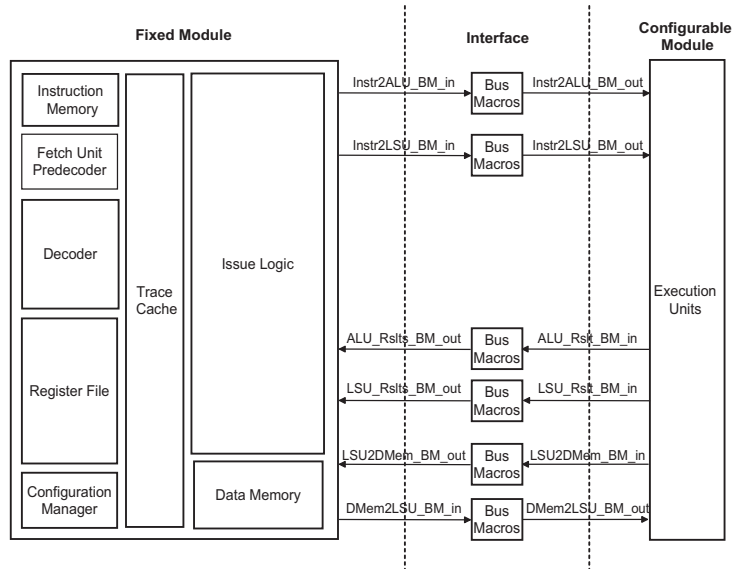
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Floorplan on a Vertex-II-XC2V8000



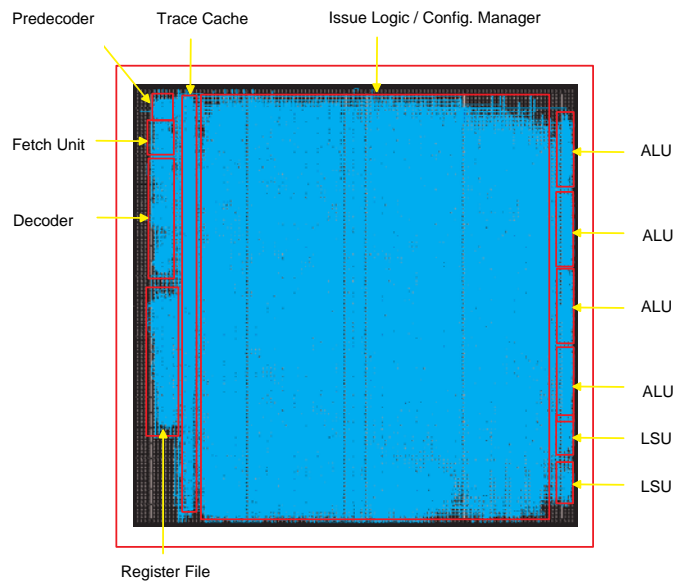
Implementation of the partial Reconfiguration



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Screenshot of the proposed processor on a Vertex-II-XC2V8000



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Conclusions



- Superscalar Technology can be improved by reconfiguration
- Legacy Code and standard compilers can be used.
- There could be a stronger improvement with fast(er) partial reconfiguration methods
- What is the difference between programming and configuration ?
- Can dynamic reconfiguration be done self-organized ?



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Thanks

... for your attention !

