

Technological Aspects for 3D FPGAs architectures with optoelectronic interconnects



seit 1548

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Technological As-
pects for 3D FPGAs
architectu-res with
optoelectronic inter-
connects

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Outline

- Why using optoelectronic interconnects for dynamically reconfigurable architectures
- State-of-the-art
- Embedded systems using dynamic optically reconfigurability
- Summary

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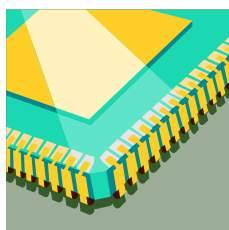
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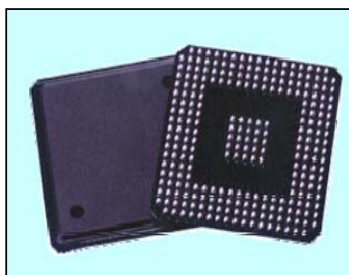
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Motivation

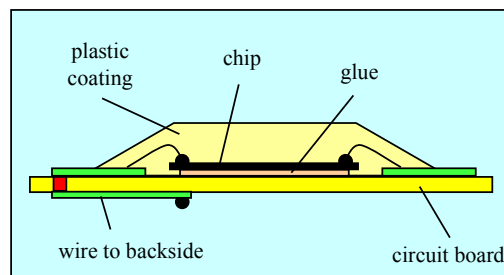
- high integration circuit technology advances
- Communication can not keep pace
 - ◆ “interconnect crisis”
 - Chip-to-chip: limited pin counts due to communication ports located at the circuit’s edge



Ball Grid Array (exterior)



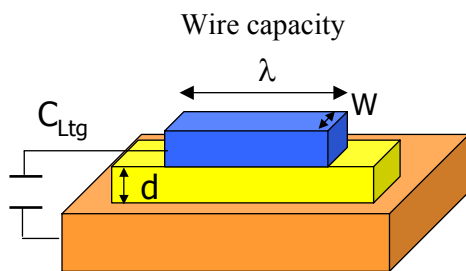
Ball Grid Array (interior)



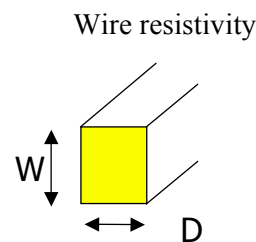
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Motivation

- on-chip: RC constant nearly immune against scaling



W: wire width d: thickness of isolation
 λ: wire length ε: material constant



D: wire thickness W: wire width
 ρ : specific resistance A = DW : cross section surface

Influence of
 scaling →

$$C = \epsilon \frac{W \cdot L}{d} \Rightarrow \epsilon \frac{W/\alpha \cdot L/\alpha}{d/\alpha} = C/\alpha$$

$$R = \rho \frac{L}{A} = \rho \frac{L}{D \cdot W} \Rightarrow \rho \frac{L/\alpha}{D/\alpha \cdot W/\alpha} = R \cdot \alpha$$

Signal propagation delay

$$t_d = R_{Ltg} C_{Ltg} L^2/2$$

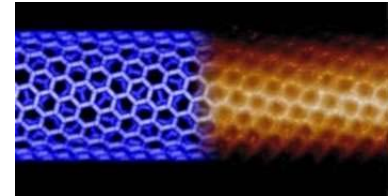
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Motivation

■ Can optics help?

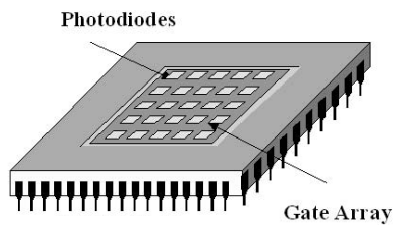
- ◆ in principle: benefits of optics
 - high time bandwidth (per channel > 1 GHz)
 - high space bandwidth (> 1000 channels/cm²)

- ◆ On-chip: at the moment, I don't believe
 - maybe: optical carbon nanotubes

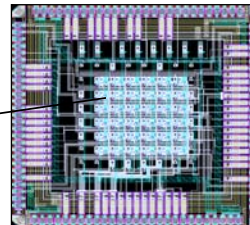


Source: <http://people.vanderbilt.edu/~tobias.hertel/>

- ◆ Chip-to-chip:
 - Optics is one solution for that problem
 - in general: 3D setup technologies



Smart pixel array



Source: FhG-IZM, Berlin

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Motivation

■ Using optical interconnects

- ◆ Clock distribution
- ◆ Broadcast and multi-point interconnections
- ◆ Pin limitation
- ◆ fast dynamic reconfiguration
 - clock-by-clock reconfiguration

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State of the art

- Mostly: optics or optoelectronics is used for more-or-less static optically connected multiprocessors
 - ◆ fiber ribbons to connect optically multiple processing nodes
 - InfiniBand, Myrinet offer optical links
 - ◆ Storage Area Networks
 - Fibre channel
 - ◆ Efforts at Intel “Fiber-to-the-processor”
 - Parallel Wavelength Division Multiplexing to overcome memory bottlenecks
 - ◆ in general:
 - The shorter the distance and the lower the desired latency or the higher the bandwidth shall be optics is better than electronics

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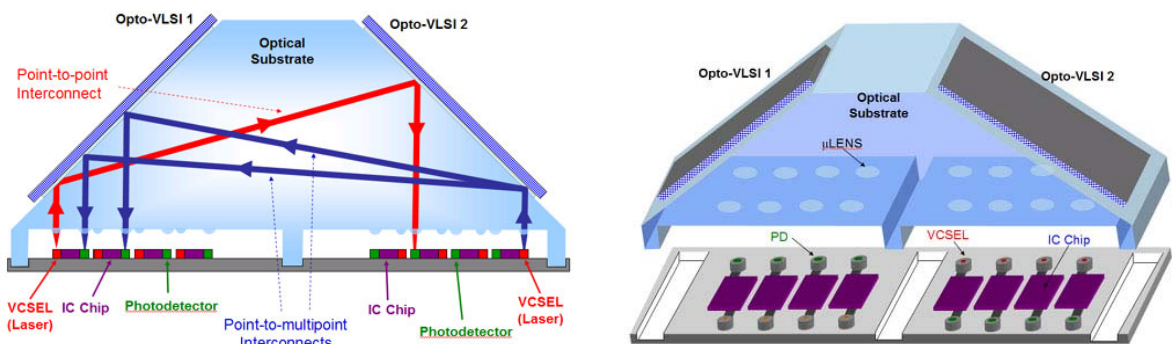
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State of the art

- Principle idea of reconfigurable optical interconnects
 - ◆ Using electrically controlled **diffractive optical elements** generating holograms for steering / splitting optical beams



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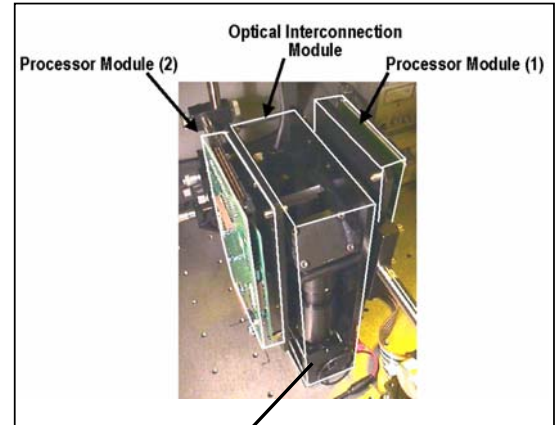
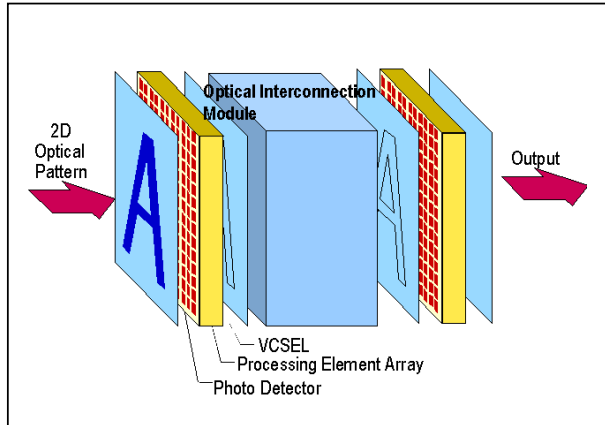
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Source: <http://comps.ecu.edu.au/>
COMPS - Western Australia Centre for Excellence for MicroPhotonic
Systems, part of the Electron Science Research Institute (ESRI) at Edith
Cowan University in Perth, Western Australia.

State of the art

◆ OCULAR-II: dynamically reconfigurable optical interconnects [Ishikawa et.al.; University Tokio]



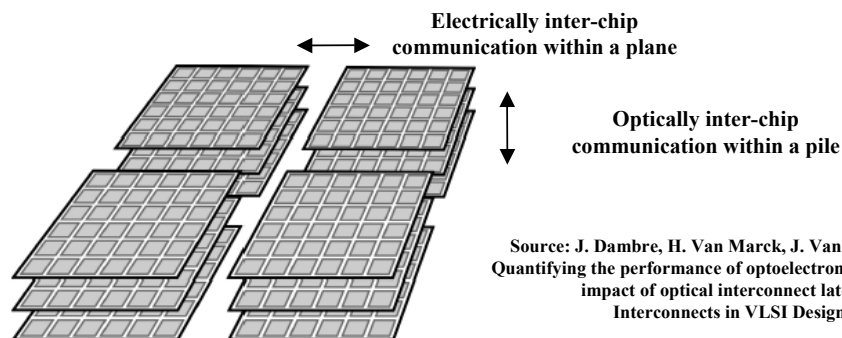
Spatial light modulators, e.g. based on LCD technique, for dynamically generated optical interconnections

State of the art

■ Optical interconnects for FPGAs

◆ Stacked OE-(optoelectronic)-FPGAs in 3D

- to reduce latency and clock frequency in multi-FPGA systems
- to increase pin number counts

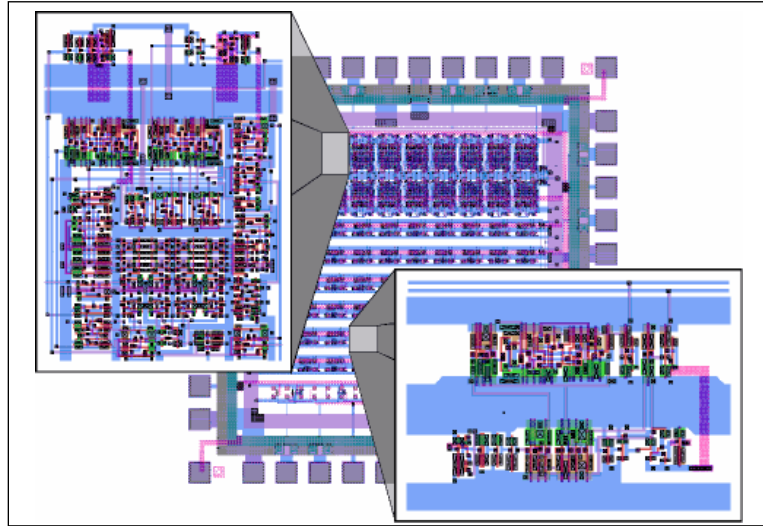


Source: J. Dambre, H. Van Marck, J. Van Campenhout
Quantifying the performance of optoelectronic FPGA's: The
impact of optical interconnect latency
Interconnects in VLSI Design

◆ increasing the utilization of CLBs by using vertical interconnects

State of the art

- mostly optics not so much used for the dynamic reconfiguration process itself
 - ◆ Optically loadable look-up-tables [Grimm, Fey 1998]
 - chip was realized in a foundry run organised by DARPA/Lucent
 - access time simulated in SPICE up to 250 MHz



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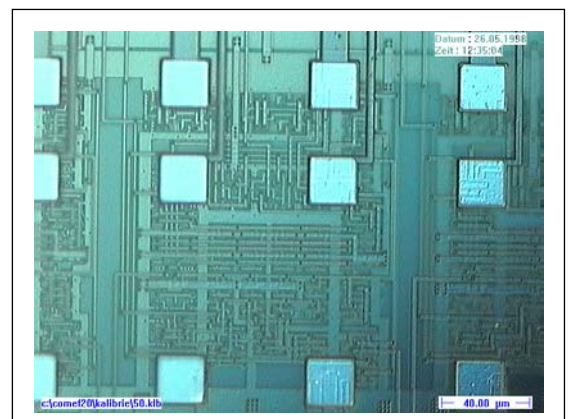
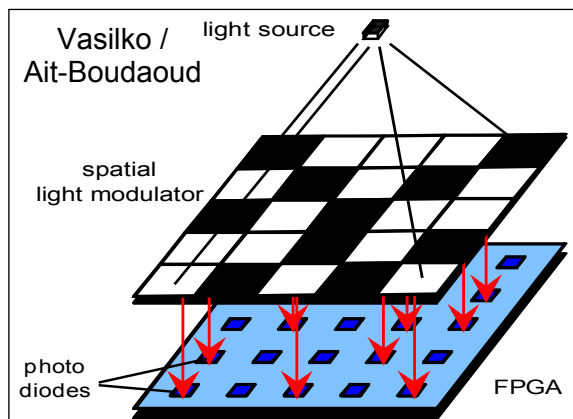
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State of the art

- ◆ parallel optical access allows fast, dynamic and partial reconfiguring
- ◆ reconfigurable look-up tables of size: 4×2 Bit
- ◆ 356 transistors on 24000µm² → ca. 4500 look-up tables / cm²
- ◆ parallel optical access allows reconfiguring of all look-up tables in ns



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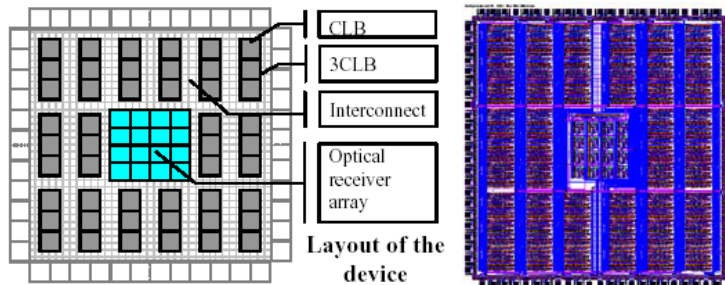
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State of the art

■ Parallel optical writing of CLBs in 2D

- ◆ Optical inputs and CLBs in the same chip plane
- ◆ Reconfiguring was not higher than with electrical writing of CLBs
- ◆ Proof-of-concept to demonstrate principal potential



Source: Leo Selavo, Steven P. Levitan and Donald M. Chiarulli
An Optically Reconfigurable Field Programmable Gate Array, 1999

◆ further works

● Optically reconfigurable gate arrays (ORGAs)

M. Miyano, M. Watanabe, F. Kobayashi, Optically Differential Reconfigurable Gate Array Using an Optical System with VCSELs, IEEE Computer Society Annual Symposium on VLSI: New Frontiers in VLSI Design (ISVLSI'05)

● ORGAs with holographic memory

J. Mumbru, G. Panotopoulos, D. Psaltis, X. An, F. Mok, S. Ay, S. Barna, and E. R. Fossum, "Optically Programmable Gate Array," Proc. SPIE -Int. Soc. Opt. Eng., vol. 4089, pp. 763-771, 2000.

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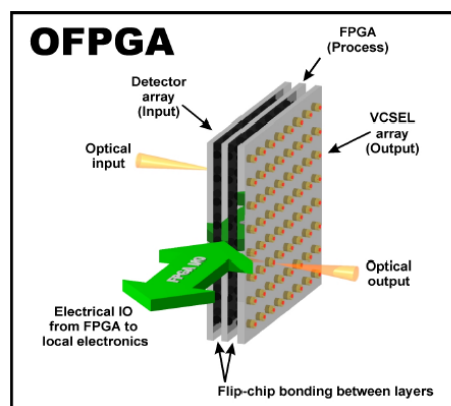
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State of the art

■ Parallel optical writing of CLBs in 3D

- ◆ Optical inputs and CLBs in neighbored flip-chipped circuit planes
- ◆ OFPGA - Proposal for an optical FPGA



Source: Keith J. Symington, John F. Snowdon and
Heiko Schroeder
High Bandwidth Dynamically Reconfigurable
Architectures using Optical Interconnects, FPL99

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Embedded systems using optical reconfigurability

■ 3D technology is fine for FPGAs

- ◆ wire lengths can be reduced
 - 50% up to 5 layers – 20% in average according to empirical analysis
- ◆ signal delay can be reduced
 - 30% up to 5 layers – 15% in average

Source: C. Ababei, P. Maidee, K. Bazargan Exploring Potential Benefits of 3D FPGA Integration, FPL2004

◆ But: must it really be optics technology?

- different technologies have to be married
- at the moment: only a hybrid concept seems promising

◆ Alternative: may be a 3D stacked electronic technology is sufficient

- Technology seems to become more and more mature
- easier to integrate with silicon electronics

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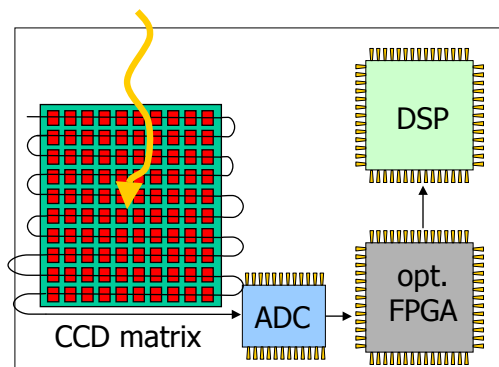
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Embedded systems using optical reconfigurability

■ FPGA integrated with optical sensor matrix is fine

- ◆ Industrial vision systems use FPGAs for fast pre-processing
- ◆ Architectures consist of optical sensor attached to FPGA
 - serial processing -> slow
 - Input / Output is bottleneck



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Embedded systems using optical reconfigurability

- Why not optical sensor array in FPGA?
 - ◆ additional layer with optical matrix
 - ◆ less components -> more compact CMOS cameras
 - ◆ less components -> cheaper at least in a middle- or long-term view
 - ◆ faster processing -> combining parallel image capturing with parallel processing
 - ◆ big market -> mass production leads to acceptable prices
 - ◆ Furthermore: use optical input also for **dynamic reconfiguration**
 - Optical interface is anyway necessary

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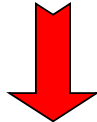
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Embedded systems using optical reconfigurability

- High-speed cameras
 - ◆ Example: resolution 640x480 pixels;
10 ms response time → 32 ns time per pixel in case of pixel-by-pixel processing
- 
- not enough for tracking analysis or motion detection
 - ◆ for a row- or column-parallel processing task improvement about 100
 - ◆ best solution: a full parallel approach
 - about 1 million instructions per pixel

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Embedded systems using optical reconfigurability

■ Functional requirements for high-speed CMOS camera

◆ 1st step: COM

- Contours / Edge detection
- Objects
- Moments

◆ 2nd step + further ones: recognition of gestures

- communication: Robot ↔ Human



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Embedded systems using optical reconfigurability

■ Top-Down-Approach

◆ necessary macro operations

- COM

◆ reduced to morphological base operations

- Erosion
- Dilation

◆ Enhancements

- Close and Open function
- Edge detection

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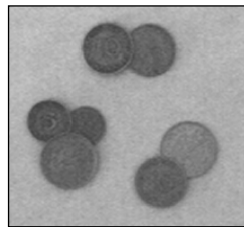
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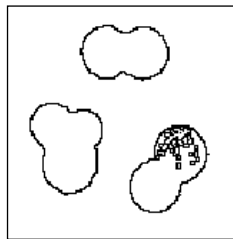
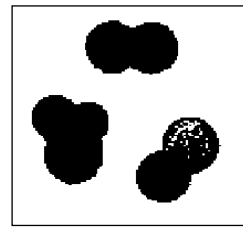
Embedded systems using optical reconfigurability

◆ Dilation, Close and Open function

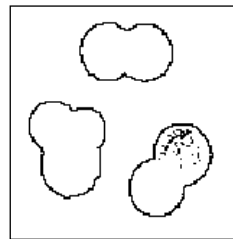
input



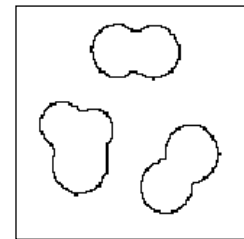
digitization



Erosion based edge detection



Dilation based edge detection



Erosion based edge detection ° Close

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Embedded systems using optical reconfigurability

◆ Erosion within direct four-pixel neighborhood

$$f_{erosion}^{(4)}(x, y) = A(x, y) \wedge A(x-1, y) \wedge A(x+1, y) \\ \wedge A(x, y-1) \wedge A(x, y+1)$$

◆ Dilation can be reduced to erosion and inverting

$$f_{dilation}^{(4)}(x, y) = A(x, y) \vee A(x-1, y) \vee A(x+1, y) \\ \vee A(x, y-1) \vee A(x, y+1)$$

$$f_{dilation}^{(4) \text{ or } (8)}(x, y) = \overline{\overline{f_{dilation}^{(4) \text{ or } (8)}(x, y)}} = \overline{f_{erosion}^{(4) \text{ or } (8)}(\bar{x}, \bar{y})}$$

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◆ Edge detection reduced to morphological operations

- $\text{Edge}(\text{IMAGE}) = \text{NOT} (\text{ERODE}(\text{IMAGE})) \text{ AND IMAGE}$

◆ *Open* and *Close* reduced to erosions and not

- $\text{Close} = \text{DILATE ERODE} = \text{NOT ERODE NOT ERODE}$
- $\text{Open} = \text{ERODE DILATE} = \text{ERODE NOT ERODE NOT}$



AND and NOT are sufficient

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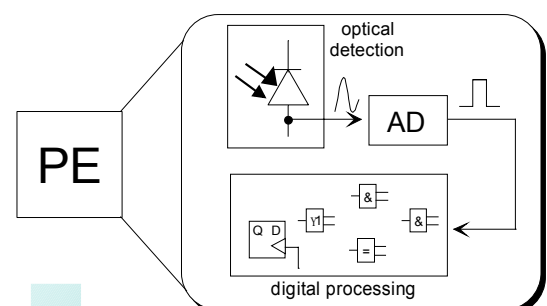
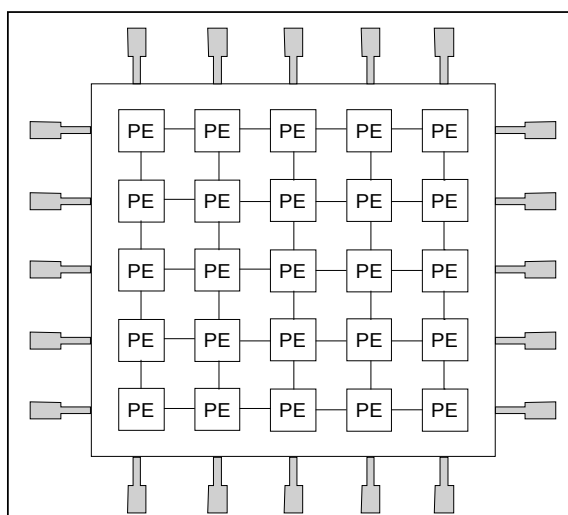
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Embedded systems using optical reconfigurability

■ SIMD (Single Instruction Multiple Data) architectures

◆ Smart pixel approach

- Pixel directly attached to a PE



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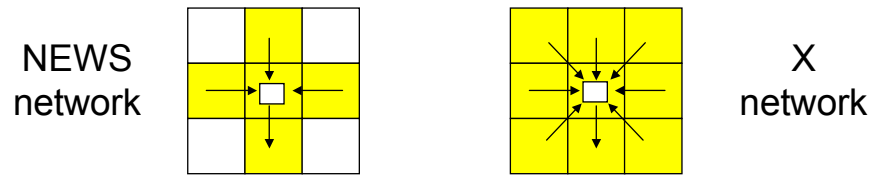
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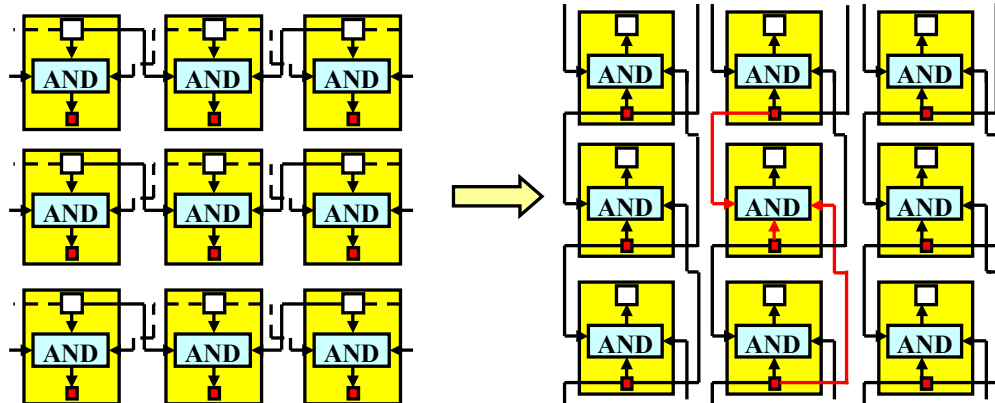
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Embedded systems using optical reconfigurability

- ◆ four-pixel or eight-point neighborhood ?



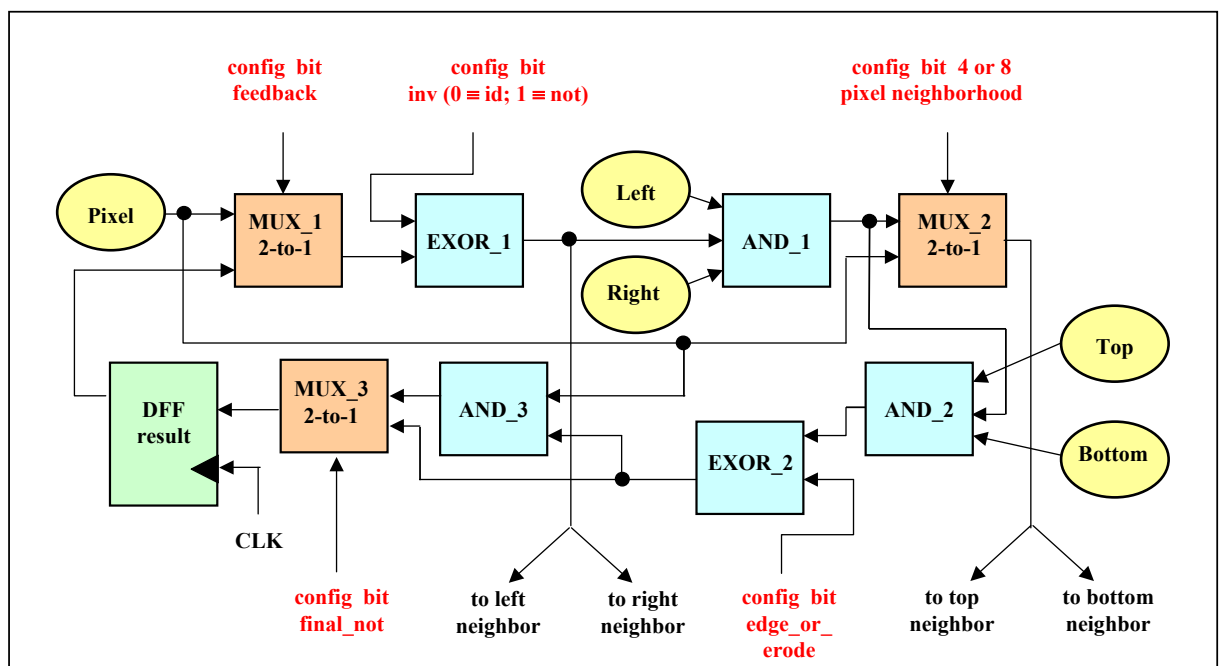
- ◆ logical AND and NEWS network



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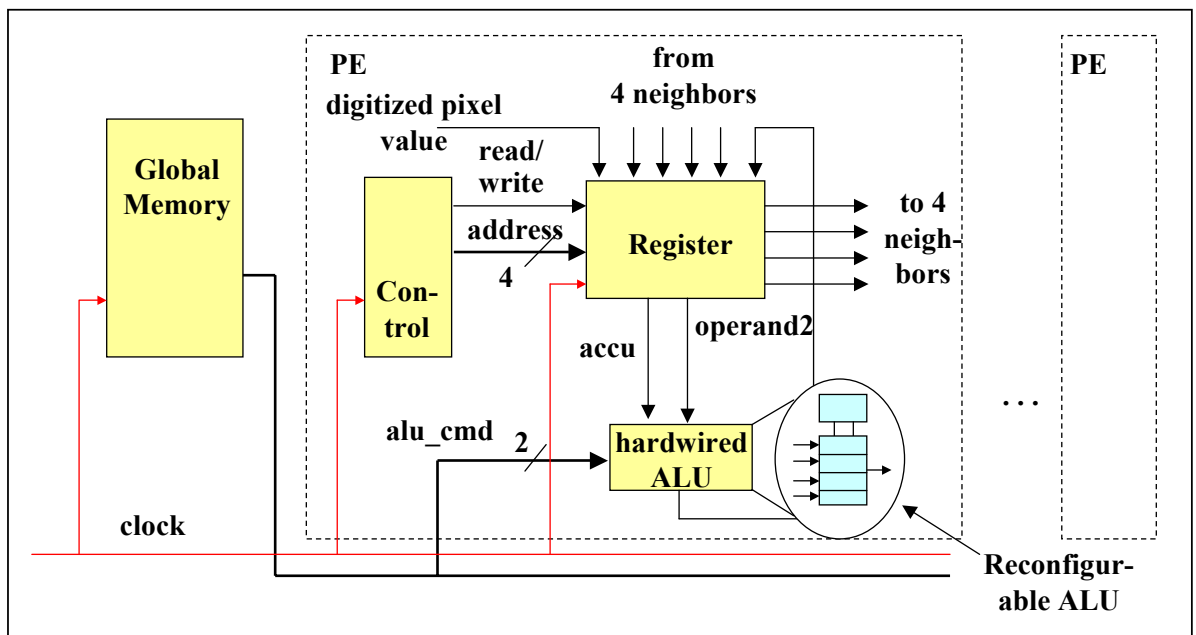
- Evaluation of three different architectures
 - ◆ PE with reconfigurable data paths



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Embedded systems using optical reconfigurability

◆ Architecture for a programmable processing element



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Embedded systems using optical reconfigurability

■ Evaluation of different architecture approaches

- ◆ Results of logic synthesis starting from SystemC for 0,35 μm CMOS process

| | Programmable PE | Programmable PE with reconfigurable ALU | Reconfigurable combinatorial PE |
|-----|------------------------|---|---------------------------------|
| PE | 43 008 μm^2 | 39 518 μm^2 | 1 722 μm^2 |
| ALU | 3 841 μm^2 | 1 396 μm^2 | 1 722 μm^2 |

- ◆ Reconfigurable combinatorial PE is the most area efficient one
- ◆ but no flexibility

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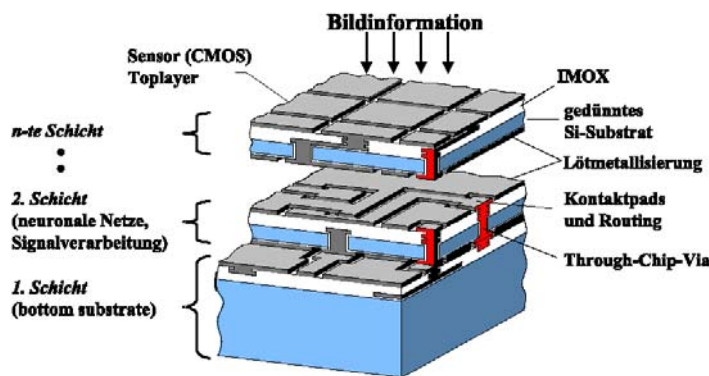
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Implementation aspects

- RC-Array as chip stack:
 - ◆ hybrid mounting technology is the promising solution
- Problems
 - ◆ Photodiodes must be on top; photo currents must be guided through the substrate
 - ◆ Mounting and assembly technology for 3D chip stacks
 - ◆ Thinning of substrate from backside



Source: M. Bschorr, H.-J. Pfeleiderer, P. Benkart, A. Kaiser, A. Munding, E. Kohn, A. Heittmann, H. Hübner, and U. Ramacher
Eine Test- und Ansteuerschaltung für eine neuartige 3D Verbindungstechnologie

Ulrich Ramacher, Wolfgang Raab, Nico Brüls, Ulrich Hachmann, Christian Sauer, Alex Schackow, Jörg Gliese, Jens Harnisch, Mathias Richter, Elisabeth Sicheneder, Rene Schöffny, Uwe Schulze, Hendrik Feldkämper, Christian Lütkemeyer, Horst Süsse, Sven Altmann
A 53-GOPS Programmable Vision Processor For Processing, Coding-Decoding And Synthesizing Of Images

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Summary

- Review of optical interconnects for reconfigurability
 - ◆ optically reconfigurable interconnects
 - ◆ optically reconfiguration of LUTs
- 3D setup technology more efficient
 - ◆ Open question if optics is the best solution for 3D setup
 - ◆ 3D stacked electronics becomes more and more mature
- Attractive application are smart optical sensors
 - ◆ OE interface is anyway necessary
 - ◆ use it for optically run-time reconfiguration
- run time reconfiguration architectures
 - higher integration density and in addition higher flexibility of smart pixels
 - Combined with 3D stacked chip setup very compact design

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